Anomalous Source-Side Degradation of InAlN/GaN HEMTs Under High-Power Electrical Stress

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Abstract— The electrical degradation of InAlN/GaN high-electron-mobility transistors for millimeter-wave applications has been examined under simultaneous high $V_{DS,stress}$ and high $I_{Dstress}$ electrical stress. Besides a drain current decrease and a positive threshold voltage shift, the creation of an anomalous source-side gate leakage path has been identified. We attribute this to high electric-field induced trap generation in the AlN layer directly under the gate edge on the source side. The resulting increase in gate leakage further exacerbates the degradation of the gate diode. In addition, we postulate that high-power stress leads to significant device self-heating that causes gate sinking and leads to a permanent positive threshold voltage shift and drain current degradation.

Index Terms— Gate sinking, high electric field, InAlN/GaN, trap generation.

I. INTRODUCTION

InAlN/GaN high-electron-mobility transistors (HEMTs) fabricated on SiC substrates have emerged as promising candidates for high-power millimeter wave applications due to their excellent gate length scaling potential [1]–[5]. With a high spontaneous polarization, a much thinner InAlN barrier layer is required in order to achieve a large enough 2-D electron gas density compared with the conventional and more mature AlGaN/GaN HEMT.

Recent technology improvements have enabled ultrascaled InAlN/GaN HEMTs with f_T of 400 GHz by minimizing parasitic effects, as reported in [6]. In addition, InAlN/GaN HEMTs with a low ohmic contact resistance of 0.36 Ω.mm have been realized and reported in [7]. What is more, well rounded InAlN/GaN HEMTs with high drain current (more than 1.2 A/mm), high breakdown voltage (73 V), and simultaneous high f_T (113 GHz) and f_{max} (230 GHz) have been reported [8]. All these results demonstrate the potential of

InAlN as a barrier material to realize ultrahigh-frequency GaN-based HEMTs for power amplifier applications.

Despite the promising properties of this novel heterostructure system, in nanometer-scale InAlN/GaN HEMTs, the use of a very thin barrier layer brings gate leakage current and reliability concerns to the fore. In this regard, the literature is very sparse.

It has been reported that in AlGaN/GaN HEMTs, under extended OFF-state stress, time-dependent defect generation in the AlGaN barrier layer can result in an increase of gate leakage even if the stress voltage is not very high [9]. In addition, recently, under forward gate stress, similar time-dependent defect generation in the gate-stack of p-GaN gate AlGaN/GaN HEMTs has been observed [10]. However, so far to our knowledge, there are no studies that have focused on the degradation mechanisms related to the gate region of InAlN/GaN HEMTs under high-power conditions. Developing an understanding of these issues is the motivation for our work.

This paper presents a study of reliability of InAlN/GaN HEMTs with emphasis on high-power stress conditions. We have observed the creation of an anomalous source-side gate leakage path. This is in contrast to the commonly observed drain-side degradation in GaN HEMTs [11]–[13]. Temperature-dependent studies as well as positive gate stress experiments have allowed us to separately identify two permanent degradation mechanisms associated with this: defect generation and gate sinking. Our research should be instrumental in realizing the potential of InAlN/GaN HEMTs in high-frequency applications.

II. DEVICES AND EXPERIMENTS

The devices studied here are industrially prototyped InAlN/GaN HEMTs with $L_G = 40$ nm fabricated on a SiC wafer [14]. Enhancement-mode operation is achieved through gate recessing of the entire InAlN layer leaving only a 1-nm AlN barrier between the channel and the gate metal. Gate to source and gate to drain distances are both 1 μm. Fig. 1 shows the cross-sectional schematic of the devices.

Our previous work suggests that these devices experience the most severe degradation under ON-state stress [14]. In this regard, for this paper, we have carried out accelerated ON-state high-power stress experiments under simultaneous high $V_{DS,stress}$ and $I_{Dstress}$ conditions which emulate the quiescent bias point in a power amplifier application. A typical
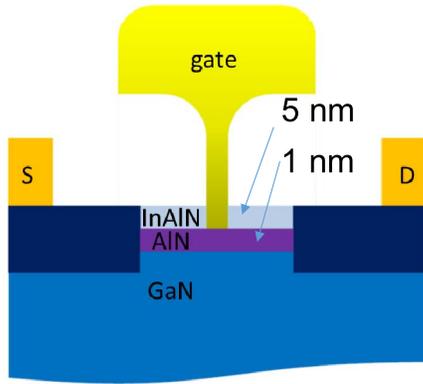
Fig. 1. Cross-sectional view of a device. $L_g = 40$ nm. Gate to source and gate to drain distances are both 1 μm.
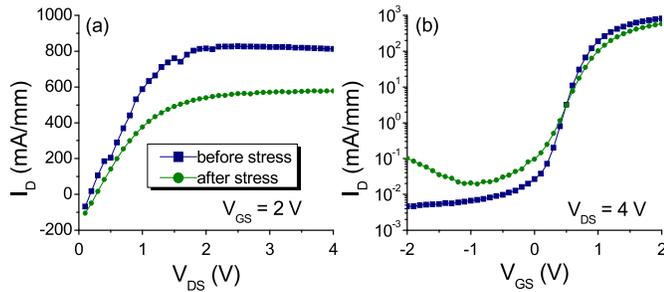
Fig. 2. RT. (a) Output and (b) transfer characteristics of a device before and after constant stress at $V_{DSstress} = 25$ V and $I_{Dstress} = 400$ mA/mm at RT. The device was thermally detrapped before and after stress. Nonzero I_D at zero V_{DS} (a) is due to gate current. We have verified this by comparing I_D and I_G. A large I_D decrease and a positive V_T shift are observed after stress. Also, a significant OFF-state drain leakage current increase is induced by stress.

example is shown in Fig. 2 that graphs (a) output (at $V_{GS} = 2$ V) and (b) transfer (at $V_{DS} = 4$ V) $I-V$ characteristics of a device before and after constant stress at $V_{DS,stress} = 25$ V and $I_{Dstress} = 400$ mA/mm for 5 min at room temperature (RT) [15]. The estimated junction temperature, according to the thermal model provided by our industrial collaborator, is $T_j = 136$ °C. $V_{GS,stress}$ was around 1.5 V but was allowed to change during the experiment in order to maintain the desired $I_{Dstress}$ level. The characteristics of Fig. 2 have been obtained after thermal detrapping, and therefore reflect permanent device degradation. Detailed information about our detrapping methodology can be found in [14]. Besides a significant decrease in drain current and a positive V_T shift, OFF-state drain current markedly increased after stress.

In these experiments, we also measured R_D and R_S through the gate injection method with $I_{Ginj} = 20$ mA/mm [16]. Fig. 3 shows the change in both R_D and R_S due to stress for the experiment of Fig. 2. The measurement points during stress are a reflection of recoverable and permanent degradation together, whereas the two final detrapped points to the right of Fig. 3(a) and (b) reflect only permanent degradation. R_D permanently increased by a noticeable amount. R_S, while also increased after stress, was much less affected.

Similar experiments were also carried out at a low substrate temperature with the goal of identifying the role of temperature in the observed degradation. Since we would expect less degradation under low T stress, to ensure some measurable degree
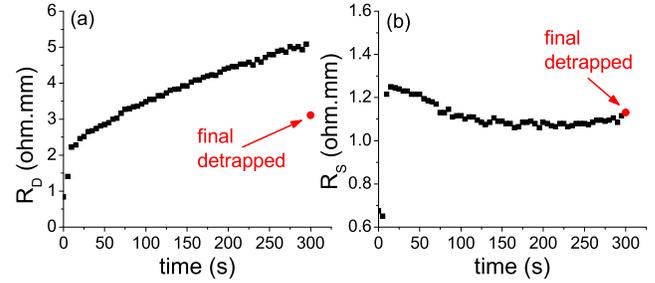
Fig. 3. Time evolution of degradation of (a) R_D and (b) R_S for the device stressed at $V_{DSstress} = 25$ V and $I_{Dstress} = 400$ mA/mm at RT. The device was thermally detrapped before and after stress. A large permanent R_D increase is observed. R_S also increased permanently but to a lesser extent compared with R_D.
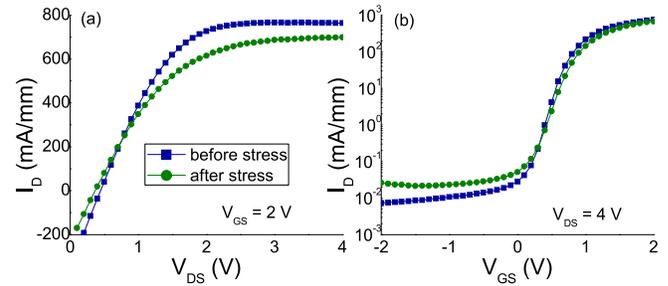
Fig. 4. RT. (a) Output and (b) transfer characteristics of a device before and after constant stress at $V_{DS,stress} = 25$ V and $I_{Dstress} = 500$ mA/mm at -50 °C. The device was thermally detrapped before and after stress. I_D decrease and positive V_T shift as well as drain leakage current increase are observed after stress. Compared with the RT experiment in Fig. 2, the overall degradation is smaller.

of permanent degradation, we increased the stress current from 400 to 500 mA/mm as we lowered the temperature.

Fig. 4 shows (a) output and (b) transfer characteristics in such an experiment before and after constant stress at $V_{DS,stress} = 25$ V and $I_{Dstress} = 500$ mA/mm with $T_{chuck} = -50$ °C (estimated $T_j = 85$ °C). $V_{GS,stress}$ was at around 1.4 V during the experiment and varied in order to maintain the designed $I_{Dstress}$ level. The lower value of $V_{GS,stress}$ required to achieve high $I_{Dstress}$, with respect to the previous experiment, reflects the negative shift of V_T that takes place as the temperature is reduced. The device in Fig. 4 showed some drain current decrease in the saturation regime and a small positive V_T shift, but much less than in the RT temperature experiment even though the stress current level is higher. The OFF-state drain current also increased due to stress. R_D and R_S both increased after stress with R_D exhibiting larger change compared with R_S, similar to what was observed in the RT experiment.

To complement this picture, Fig. 5 shows the degradation of the RT gate current for both experiments. The measurements are also performed after thermal detrapping and reflect permanent degradation. Both devices exhibit significant gate leakage increase in the reverse and low forward gate bias regimes. This indicates that a lower stress temperature only marginally reduces gate current degradation under high-power stress. This is different from the degradation signature of I_D. These and other experiments suggest two different degradation mechanisms for gate current and drain current where I_D degradation is strongly thermally enhanced and I_G degradation is less affected by temperature.
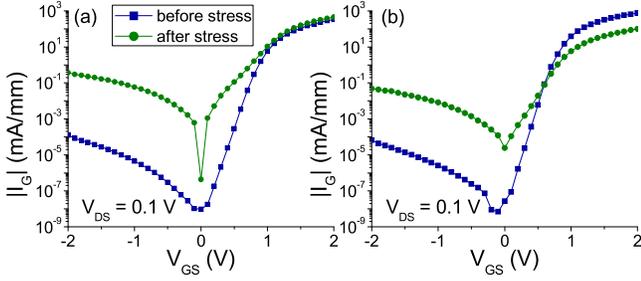
Fig. 5. RT I_G–V_{GS} plots before and after stress of the device in (a) Fig. 2 and (b) Fig. 4. The device was thermally detrapped before and after stress. I_G increased significantly in both experiments.
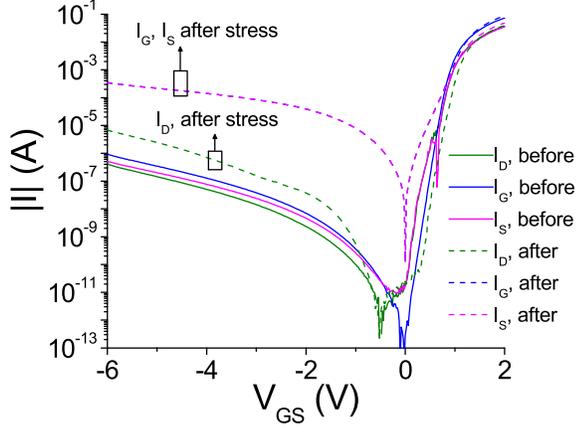
Fig. 6. I_G–V_{GS} characteristics (measured at 25 °C) at $V_{DS} = 0$ before (solid lines) and after (dashed lines) constant stress at $V_{DS,stress} = 25$ V and $I_{Dstress} = 400$ mA/mm [same experiment as in Figs. 2 and 5(a)]. I_S and I_D are also indicated. The dip in I_S at around 0.9 V is likely due to oscillations. After stress, I_G and I_S increase by several orders of magnitude. Comparatively, I_D shows a much smaller increase.

III. SOURCE-SIDE GATE LEAKAGE PATH

To better understand the origin of the gate leakage current increase after high-power stress, we have carried out three terminal current measurements and extracted the current distribution through the source and drain terminals as a function of gate voltage.

Fig. 6 shows the three terminal currents before and after stress (in both cases, the device has been thermally detrapped) for the RT stress experiment corresponding to Fig. 2. Similar to what Fig. 5(a) suggests, I_G after stress increases by several orders of magnitude. Surprisingly, I_S closely follows I_G, whereas I_D increases much less. This suggests that the gate current increase takes place through a leakage path created between the gate and the source. A similar source-side leakage increase is also observed in the low T experiment of Fig. 4 (Fig. 7). This unique degradation signature of source-side damage of the gate diode is uncommon in conventional AlGaN/GaN HEMTs [17] as well as InAlN/GaN HEMTs after ON-state stress [18].

In order to understand the origin of the observed source-side degradation, we have studied the temperature dependence of the three terminal currents before and after stress. All measurements were conducted with the device thermally detrapped first so that the extra recovery effect due to characterization temperature should be minimum. For the RT stress experiment,
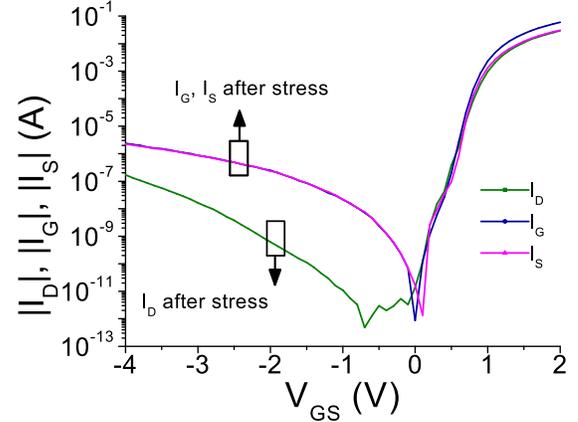
Fig. 7. I_G–V_{GS} (with $V_{DS} = 0$ V) characteristics (measured at 0 °C) at $V_{DS} = 0$ after low T (−50 °C) constant stress at $V_{DS,stress} = 25$ V and $I_{Dstress} = 500$ mA/mm [same experiment as in Figs. 4 and 5(b)]. I_S and I_D are also indicated. After stress, I_S closely follows I_G, whereas I_D is orders of magnitude lower.
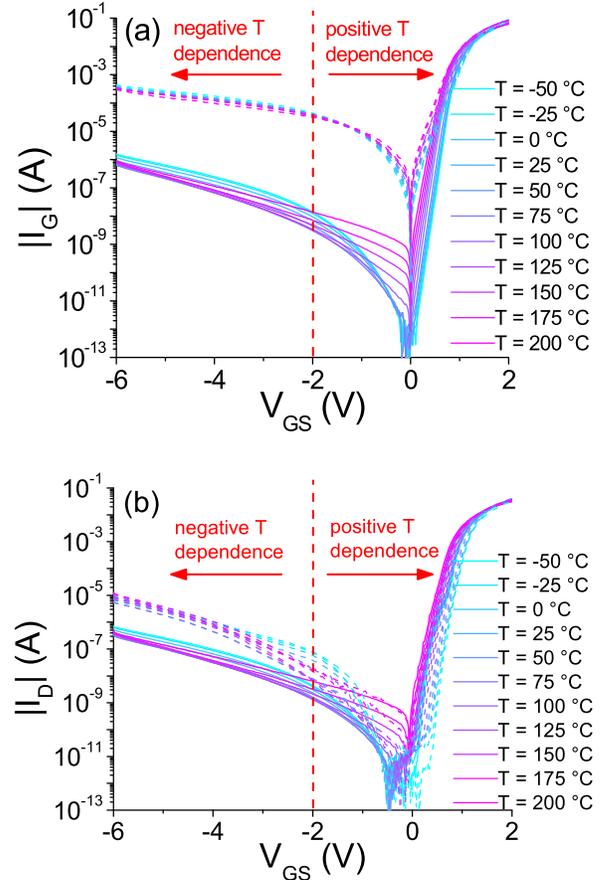
Fig. 8. (a) I_G–V_{GS} (with $V_{DS} = 0$ V) and (b) I_D–V_{GS} (with $V_{DS} = 0$ V) before (solid lines) and after (dashed lines) constant stress at $V_{DS,stress} = 25$ V and $I_{Dstress} = 400$ mA/mm [same experiment as in Figs. 2, 5(a) and 6]. The I–V sweeps were conducted at T_{chuck} from −50 °C to 200 °C in 25 °C steps.

Fig. 8(a) and (b) shows I_G and I_D, respectively, for T_{chuck} from −50 °C to 200 °C in 25 °C steps before (solid lines) and after (dashed lines) stress. I_S behaves similar to I_G and is not shown here.

From Fig. 8(a), before stress, there is an overall positive temperature dependence over most of the voltage range. This suggests a thermionic or thermionic field emission

dominated charge transport mechanism for the gate diode on both source and drain sides. For high reverse regime ($V_{GS} < -2$ V), on the other hand, $|I_G|$ exhibits a negative temperature dependence. This could be due to drift-limited current transport in the access regions of the device.

Stress has a significant impact on the T dependence of the currents in all three regimes for I_G and I_S, much less so for I_D. As shown by the dashed lines in Fig. 8(a), a significantly reduced temperature dependence is observed in all three regimes for I_G and I_S, indicating a dominance of electron tunneling. This posits a possible explanation to the source-side degradation: the formation of defects in the AlN layer on the source side, leading to significantly increased trap-assisted conduction mechanisms, such as trap-assisted-tunneling or Poole–Frenkel emission. Our later studies reveal that the increased gate current on the source side can be well explained by the Poole–Frenkel emission [19]. The drain side of the gate diode is less affected due to the reverse bias prevalent there under high-power conditions. I_D, as a result, more or less retains its temperature dependence [Fig. 8(b)]. Similar results have been observed in the sample subjected to low-temperature stress.

IV. DISCUSSION

From these and similar experiments, two main degradation mechanisms can be distinguished, most likely of different physical origins. In the first place, under high $V_{DS,stress}$ and $I_{Dstress}$, the gate–source diode is strongly forward biased and there is significant gate current. For the RT experiment shown in Fig. 2, $I_{Gstress}$ increased from about 10 to 50 mA/mm and similarly for the low T experiment shown in Fig. 4, $I_{Gstress}$ increased from about 20 to 45 mA/mm. The combination of high gate current, and high forward gate voltage, and therefore the strong electric field across the 1-nm AlN barrier on the source side generates defects in the AlN. Similar defect formation has been observed in the AlGaN/GaN system under strong reverse bias conditions [9] and also in AlGaN/GaN devices with p-GaN gate under forward bias stress [10]. On the drain side of the gate, the field across the AlN barrier is reversed and is most likely smaller due to the appearance of a depletion region in the access region next to it. This results in much less degradation compared with the source side.

A second mechanism is strongly thermally enhanced. It arises as a result of high temperature due to device self-heating associated with high-power dissipation ($V_{DS,stress} \times I_{Dstress}$) in the device. On top of this, local device self-heating due to significantly increased gate leakage current might also occur. All this results in a positive V_T shift and a reduction in I_{Dmax} [20]–[22]. The observed R_D increase is also consistent with the positive V_T shift, since after stress, the increased resistance associated with the intrinsic channel starts to play a nonnegligible role in the extraction of R_D through the current injection method.

Our defect generation hypothesis suggests that a similar degradation should take place under forward gate bias stress under $V_{DS} = 0$ V conditions if the electric field and temperature are high enough, except that in this case, the degradation should occur in a symmetric way.
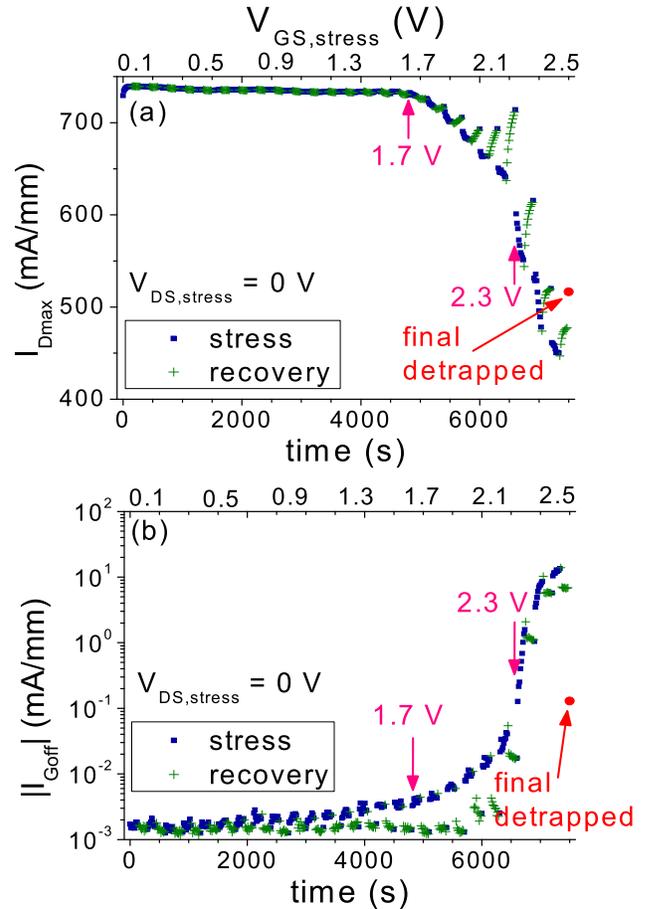
Fig. 9. Degradation of (a) I_{Dmax} (at $V_{GS} = 2$ V and $V_{DS} = 4$ V) and (b) $|I_{Goff}|$ (at $V_{GS} = -2$ V and $V_{DS} = 0.1$ V) as a function of stress time in a step-stress-recovery experiment with $V_{Gstress} > 0$ and $V_{DS} = 0$. I_{Dmax} and I_{Goff} start to degrade at $V_{GS,stress}$ around 1.8 V. Enhanced degradation takes place for $V_{Gstress}$ beyond 2 V, indicating defect formation in the AlN layer. Final detrapped values are also shown as red dots indicating a permanent decrease in drain current and a permanent increase in gate leakage current.

To verify this, we conducted a step-stress-recovery experiment at RT with source and drain grounded and positive $V_{GS,stress}$ increasing from 0.1 to 2.5 V in 0.1 V steps. The stress time during each step was 5 min. Fig. 9 shows the evolution of I_{Dmax} and I_{Goff} with time during stress.

We observe that I_{Dmax} reduction [Fig. 9(a)] and I_{Goff} increase [Fig. 9(b)] start at around $V_{GS,stress} = 1.7$ V. This corresponds to the onset of defect formation in the AlN layer. As stress continues, a significant acceleration of I_{Goff} degradation occurs when $V_{GS,stress}$ exceeds $\sim$2.3 V. Also, fast I_{Dmax} decrease and R_D and R_S increase (not shown) take place at the same time, indicating a second degradation mechanism kicking in.

To make the overall picture clearer, the time evolution of the gate current during stress is shown in Fig. 10. Before $V_{GS,stress}$ reaches 2.3 V, for constant stress, $I_{Gstress}$ decreases with time which is the typical signature of electron trapping. When $V_{GS,stress}$ exceeds 2.3 V, at constant stress, the $I_{Gstress}$ behavior changes significantly and starts to increase with time. This marks the onset of the second degradation mechanism. The signature of this mechanism is enhanced I_{Goff} leakage,
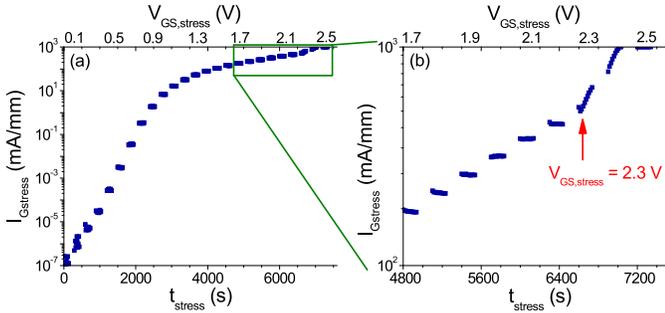
Fig. 10. (a) Time evolution of $I_{Gstress}$ (at $V_G = V_{GS,stress}$ and $V_{DS,stress} = 0$ V) as $V_{GS,stress}$ increases from 0.1 to 2.5 V in 0.1 V steps. (b) Zoomed-in view of (a) for $V_{GS,stress}$ ranging from 1.3 to 2.5 V. Before $V_{GS,stress}$ reaches 2.3 V, $I_{GStress}$ decreases with time for each $V_{GS,stress}$ level, possibly due to electron trapping. As $V_{GS,stress}$ exceeds 2.3 V, $I_{Gstress}$ exhibits an observable increase with time, indicating gate-stack degradation.
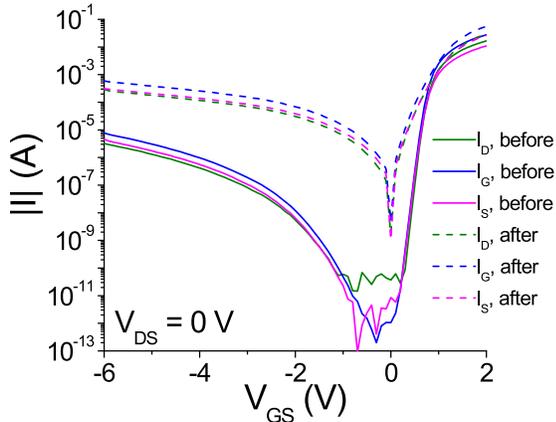
Fig. 11. I_G–V_{GS} characteristics at $V_{DS} = 0$ before (solid lines) and after (dashed lines) positive V_{GS} step-stress-recovery experiment of Figs. 9 and 10 with $V_{DS} = 0$. I_S and I_D are also indicated. After stress, I_G roughly splits in half between I_D and I_S indicating degradation of both source and drain sides of the device.

I_{Dmax} decrease, as well as R_D and R_S increase (not shown). This degradation pattern is similar to that observed under prolonged high-power stress discussed previously and is believed to be related to device self-heating induced Schottky gate degradation, possibly gate sinking.

Unlike in the high-power stress experiments before, the three terminal current measurements for this device show that the permanent increase in I_G after stress splits roughly in half through the source and drain (Fig. 11). This means that the degradation is symmetric along the gate, just as expected.

In order to verify the gate sinking hypothesis, we carried out cross-sectional structural analysis with TEM on both virgin devices and stressed devices. Fig. 12 shows HR-TEM images of the intrinsic gate regions of three devices: Fig. 12(a) is a virgin device, Fig. 12(b) is the device stressed under high-$V_{DS,stress}$-high-$I_{Dstress}$ condition discussed previously (Fig. 2), and Fig. 12(c) is a device stressed under positive step-V_{GS} condition with $V_{GS,stress}$ increasing from 0 to 2.5 V ($V_{DS,stress} = 0$ V), similar to the experiment shown in Figs. 9 and 10 except that the stress temperature was $T_{stress} = 150$ °C instead of RT. This device exhibits a degradation pattern of the second degradation mechanism tentatively attributed to gate sinking. That is, a significantly increased I_{Goff}, a decreased I_{Dmax}, as well as
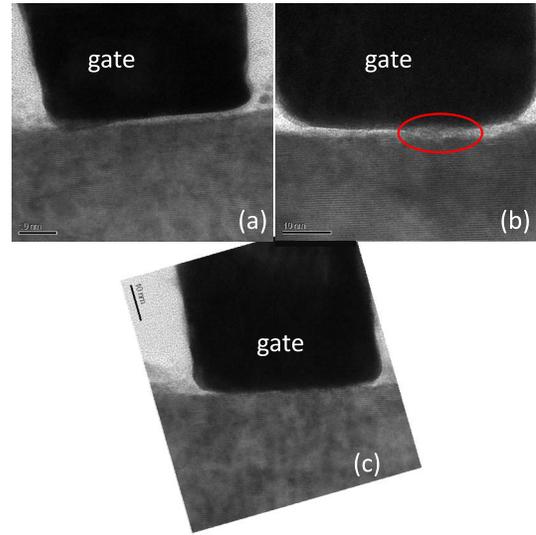
Fig. 12. HRTEM cross-sectional image of intrinsic gate region of three devices. (a) Virgin device. (b) Device stressed under high-$V_{DS,stress}$-high-$I_{Dstress}$ condition as in Fig. 1. (c) Device stressed under high T (150 °C) positive $V_{GS,stress}$ condition with $V_{DS} = 0$. For all three figures, the device source is on the left side of the gate and the drain is on the right side.
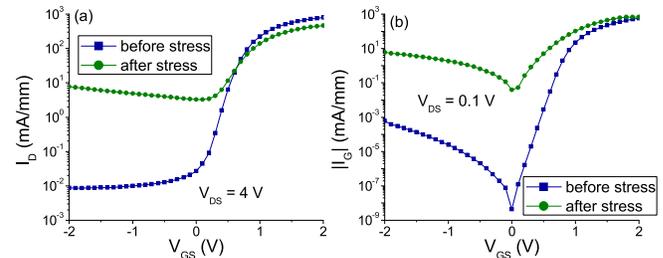
Fig. 13. (a) Transfer and (b) gate current characteristics of device before and after high T positive step-V_{GS} stress. Measurements after the device were thermally detrapped. I_{Dmax} decrease and I_{Goff} increase are observed after stress. The subthreshold characteristics are severely degraded. Excessive gate leakage current after stress makes the threshold voltage extraction not accurate.

increased R_D and R_S. Fig. 13 shows the transfer (a) and gate current (b) characteristics of this device before and after stress. Permanent degradation for this device is more severe than the device stressed under high-$V_{DS,stress}$-high-$I_{Dstress}$ condition at RT (Fig. 2).

Interestingly, for both the virgin device (a) and the device stressed under high-$V_{DS,stress}$-high-$I_{Dstress}$ condition (b), there is a light region between the gate metal and the underlying semiconductor layer. From electron energy loss spectroscopy (EELS) analysis, we have confirmed that the light region corresponds to some oxide species. This is likely due to the oxidation of AlN interlayer during the gate recess step and should then exist in all devices. We have verified this in two other virgin samples. The native oxide layer appears to be nonuniform, as suggested by the disappearance of the light region in Fig. 12(a) toward the left corner. This could be due to process variations or imaging artifact. A similar thin native oxide layer at the semiconductor/metal interface with uneven consistency has been reported also in AlGaN/GaN HEMTs in the past [23].

For the device stressed under high T and harsh $V_{GS,stress}$ condition with $V_{DS,stress} = 0$ V, Fig. 12(c) shows that the oxide

layer seems to have been almost completely consumed over most of the gate area. This is similar to what has previously been observed in AlGaN/GaN HEMTs after high electric field stress at high temperature [21], [22]. This most likely is the gate sinking mechanism postulated above. The reduction of the interfacial oxide would shift V_T positive and result in a large increase in I_G. This positive V_T shift will then result in decreased I_{Dmax} due to a reduction in gate overdrive. The R_D and R_S increases are also most likely associated with the V_T shift since the measured resistance through the gate-current injection technique includes half of the channel resistance. In an enhancement-mode device, this can increase significantly as V_T shifts positive.

Fig. 12(b), for the sample stressed under high-power conditions, shows the partial consumption of the light oxide layer in the region highlighted by the red circle. EELS line scans at three locations across the device gate verified that in the red circled area the interfacial oxide layer is the thinnest. This incomplete consumption of native oxide layer, as compared with the more complete dissolution in Fig. 12(c), is consistent with the lower degree of overall permanent electrical degradation observed in this device. From an electrical point of view, oxide consumption is equivalent to gate sinking. We then expect it to take place in the entire device channel, if not more toward drain side. The previously discussed source side degradation, which is a result of defect generation, is not observable under TEM imaging.

V. Conclusion

In summary, two distinct degradation mechanisms are revealed in our study. We have identified an anomalous source-side gate degradation in InAlN/GaN HEMTs stressed under simultaneous high V_{DS} and high I_D conditions. We have found that a strong positive bias on the gate coupled with self-heating leads to a significant increase in gate leakage current that flows through the source side of the device. We attribute this to defect formation in the AlN barrier driven by high electric field and high temperature, coupled with gate sinking. Our study should be instrumental in aiding the development of reliable scaled InAlN/GaN HEMTs.

Acknowledgment

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